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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,452	06/29/2001	Barbara D. Kotzias	42233/MJM/A717	1589

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EXAMINER

GRAYBILL, DAVID E

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/896,452	KOTZIAS ET AL.
	Examiner	Art Unit
	David E Graybill	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 29 June 2001.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-24 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

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The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 22, there is insufficient antecedent basis for the phrase, "each of said semiconductor die."

In the rejections infra, reference labels are generally recited only for the first recitation of identical language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 10-17, 19-22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Davis (5214307).

At column 1, lines 54-56 and 62-63, column 2, lines 37-45, and column 3, line 55 to column 4, line 37, Davis teaches the following:

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1. A method for joining a semiconductor die to a leadframe comprising the steps of: providing a semiconductor die 14 and a leadframe 40; forming at least three pedestals 42 raised above a surface of said leadframe in a mounting area adapted for receiving said semiconductor die attached thereto, each of said pedestals having substantially the same pedestal height; introducing an adhesive material 20 onto said mounting area, said adhesive material including an average thickness being at least as great as said pedestal height; and joining said semiconductor die to said mounting area such that said semiconductor die contacts each of said pedestals and said adhesive material.
3. The method as in 1, in which said adhesive material comprises an epoxy.
4. The method as in 1, in which said adhesive material comprises a thermally curable epoxy and said step of joining includes heating to cure said epoxy.
5. The method as in 1, in which said pedestals each include a height within the range of 1-2 mils.
6. The method as in 1, wherein said leadframe is formed of a malleable material and said step of forming comprises mechanically stamping said leadframe to form said pedestals as

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integral portions of said leadframe which protrude from said surface.

7. The method as in 1, in which each of said pedestals includes a shape being one of cylindrical and conical.

10. A method for joining a semiconductor chip to a leadframe comprising the steps of: providing a leadframe and a semiconductor chip; forming at least three pedestals raised above a surface of said leadframe in a mounting area adapted for receiving said semiconductor chip attached thereto, each of said pedestals having substantially the same pedestal height; introducing a viscous solder material 20 onto said mounting area; and joining said semiconductor chip to said mounting area of said leadframe such that said semiconductor chip contacts each of said pedestals and said solder.

11. An assembly comprising a semiconductor die attached to a surface of a leadframe by an adhesive, said leadframe including at least three pedestals one of protruding from and formed over said surface, each of said pedestals having substantially the same pedestal height, and said semiconductor die contacting each of said pedestals.

12. The assembly as in 11, in which said pedestal height lies within the range of 1-2 mils.

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13. The assembly as in 11, in which said pedestals each include a top portion which contacts said semiconductor die and said top portion includes an area 2 within the range of 490 micron<sup>2</sup> and 2000 micron<sup>2</sup>.

14. The assembly as in 11, in which each of said pedestals are conical in shape and include a base coincident with said surface and an apex which contacts said semiconductor die.

15. The assembly as in 11, in which said semiconductor die includes an area which lies within the range of 256 mils<sup>2</sup> to 1 inch<sup>2</sup>.

16. The assembly as in 11, wherein said pedestals each comprise raised portions of said leadframe.

17. The assembly as in 11, wherein each of said pedestals are discrete members joined to said surface.

19. The assembly as in 11, wherein said adhesive comprises an epoxy.

20. The assembly as in 11, wherein said pedestals are substantially cylindrical in shape and include substantially flattops which contact said semiconductor die.

21. The assembly as in 11, in which said semiconductor die includes an integrated circuit formed thereon [inherently], an opposed bottom surface contacting said adhesive and said

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pedestals and facing said leadframe, and sides, and said adhesive extends at least partially up said sides.

22. The assembly as in 11, in which said adhesive laterally surrounds each of said pedestals and is interposed between said semiconductor die and said surface, has a thickness substantially equal to said pedestal height, and therefore contacts and adheres to each of said semiconductor die and said leadframe.

24. The assembly as in 22, in which said adhesive is characterized as being void-free between said semiconductor die and said surface.

To further clarify the teaching that the pedestals are substantially cylindrical in shape and the particular claimed dimensions, it is noted that, as cited, Davis teaches that the bumps can be any height, size and shape.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 8, 9, 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis (5214307).

Davis is applied for the same reasons it was applied to claims 1, 3-7, 10-17, 19-22 and 24. In addition, Davis teaches the following:

8. The method as in 1, in which said step of providing includes providing said semiconductor die having a top, sides, and a bottom for contacting said pedestals, and in which said step of introducing includes introducing a deformable adhesive material to a sufficient thickness such that said step of joining urges portions of said adhesive material to extend at least partially

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along said sides of said semiconductor die when said bottom contacts said pedestals.

9. The method as in 1, in which said step of joining includes joining a bottom surface of said die to said leadframe such that said bottom surface contacts each of said pedestals.

said leadframe such that said bottom surface contacts each of said pedestals.

23. The assembly as in 22, in which said semiconductor die includes a top surface, an opposed bottom surface contacting said adhesive and said pedestals and facing said leadframe, and sides, and said adhesive extends at least partially up said sides.

However, Davis does not appear to explicitly teach the following:

2. The method as in 1, further comprising the step of heating to urge said adhesive material to deform and in which said step of joining includes urging said adhesive material to solidify.

8. The method as in 1, in which said step of providing includes providing said semiconductor die having a top including a semiconductor device formed thereon.

9. The method as in 1, in which said semiconductor die includes an integrated circuit formed on a top surface thereof.

18. The assembly as in 11, wherein said leadframe is formed of copper.

23. The assembly as in 22, in which said semiconductor die includes a top surface including circuitry thereon.

Nonetheless, Davis teaches that the adhesive material is solder, and official notice is taken that it is well known to heat solder to urge it to deform and that solder joining includes urging solder to solidify. Moreover, it would have been obvious to combine the well known process with the process of Davis because it would enable joining.

Also, official notice is taken that it is well known to provide a semiconductor die having a top including a semiconductor device formed thereon and an integrated circuit formed on a top surface thereof. Moreover, it would have been obvious to combine the well known process with the process of Davis because it would provide a semiconductor die.

Official notice is also taken that it is well known to provide a leadframe formed of copper. Furthermore, it would have been obvious to combine the well known process with the process of Davis because it would provide a leadframe.

The prior art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It

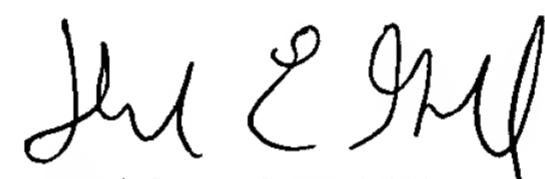
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is cited primarily to show inventions similar to the instant invention.

***Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.***

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.



David E. Graybill  
Primary Examiner  
Art Unit 2827

D.G.  
17-Jun-02